Montium® Reconfigurable Digital Signal Processing Tile Processor (TP)

Product Brief

Features

Reconfigurable Processing Part Array
- 5 processing parts (e.g., 16-bit).
- 10 parallel single-port memories (e.g., 2 Kbyte).
- Signed and fixed-point arithmetic.
- Processing performance of an ASIC.
- Low power (e.g., 0.1 – 0.5 mW/MHz in 0.13 μm CMOS).
- Low cost by virtue of tiny core (e.g., 2 mm² in 0.13 μm CMOS).

Reconfigurable Technology
- Programmability of a DSP.
- Small configuration file (typically < 1 Kbyte).
- Ultra fast configuration time (< 5 μs).
- Datapath switchable on a cycle-by-cycle basis.

Configurable Soft Core
- Completely configurable RTL soft core
  - memory capacity, datapath width, configuration registers and decoder sizes.
- Extremely versatile building block
  - accelerator core for general purpose processor.
  - large multi-core systems-on-chip.

Communication and Configuration Unit
- Supports streaming and frame based communication.
- High speed communication with:
  - industry standard interfaces.
  - proprietary interfaces.
  - NoC (network-on-chip).

Performance Benchmarks
- 1024-point FFT/IFFT: 5140 cycles
- 25-tap FIR filter (no. samples=512): 2562 cycles
- 32×32 matrix product: 8192 cycles
- 32×32 matrix-vector product: 256 cycles

Recore Systems BV
PO Box 77
7500 AB Enschede
The Netherlands
℡ +31 53 4753 000
℡ +31 53 4753 009
@ info@recoresystems.com

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