Features

Reconfigurable Processing Part Array
- 5 processing parts (e.g., 16-bit).
- 10 parallel single-port memories (e.g., 2 Kbyte).
- Signed and fixed-point arithmetic.
- Processing performance of an ASIC.
- Low power (e.g., 0.1 – 0.5 mW/MHz in 0.13 \( \mu \)m).
- Low cost by virtue of tiny core (e.g., 2 mm\(^2\) in 0.13 \( \mu \)m).

Reconfigurable Technology
- Programmability of a DSP.
- Small configuration file (typically < 1 Kbyte).
- Ultra fast configuration time (< 5 \( \mu \)s).
- Datapath switchable on a cycle-by-cycle basis.

Configurable Soft Core
- Completely configurable RTL soft core
  - memory capacity, datapath width, configuration registers and decoder sizes.
- Extremely versatile building block
  - accelerator core for general purpose processor.
  - large multi-core systems-on-chip.

Communication and Configuration Unit
- Supports streaming and frame based communication.
- High speed communication with:
  - industry standard interfaces.
  - proprietary interfaces.
  - NoC (network-on-chip).

Applications
- Wireless communication systems for cell phones and base station applications.
- Digital radio for terrestrial and satellite applications.
- Digital TV receivers for fixed and mobile applications.
- Image processing applications.
- Speech and audio signal processing algorithms.
- Radar signal processing applications, such as tracking algorithms and adaptive beam forming applications.
- Biomedical signal processing applications.

Functional block diagram

Performance Benchmarks
- 1024-point FFT/IFFT 5140 cycles
- 25-tap FIR filter (no. samples=512) 2562 cycles
- 32\( \times \)32 matrix product 8192 cycles
- 32\( \times \)32 matrix-vector product 256 cycles

Normalized performance for 1024 point FFT.