Highlights

- N-point DCT / IDCT / MDCT / IMDCT for $N = 2^3, 4, \ldots, n$
  (maximal length depends on memory size of used Montium configuration)
- High-efficiency parallel processing
- Fixed-point arithmetic with selectable word width
- Efficient streaming I/O
- Low power consumption
- Low cost
- Single Montium core implementation
- Reprogrammable alternative for hardware accelerators

Overview

The Montium® (M)DCT IP core is a collection of parametrized kernels realizing discrete cosine transforms of various types and sizes. Implemented in MontiumC, the Montium (M)DCT IP core requires an extremely low number of clock cycles in order to compute DCTs, IDCTs, MDCTs and IMDCTs on fixed-point data blocks up to lengths of several Kwords. As an example, a 2048-point IMDCT typically used in MPEG Advanced Audio Coding requires just 4378 cycles, or 44 μs when clocked at 100MHz.

Montium IP core

Recore's Montium is a dynamically reconfigurable IP core for computation intensive DSP algorithms. The Montium can be used as part of heterogeneous multi-core system-on-chip or as an accelerator core for microprocessor based systems. High performance coupled with excellent power efficiency is achieved by virtue of the Montium tile processor's unique coarse-grained reconfigurable architecture.

Sensation Suite IDE

Based on the industry standard Eclipse platform, the Sensation Suite is an integrated development environment (IDE) for Montium based platforms. The comprehensive IDE is an all-in-one compiler, simulator, debugger and editor, enabling easy application development with the Montium (M)DCT IP core. The IDE also supports system level simulation using the Montium hardware development board, hence reducing time to market.

Applications

- Lossy audio / image / video compression
- Multimedia codecs (e.g. MPEG video, AAC, Dolby AC-3)
- Real-time broadcast applications (e.g. DAB, DMB, DRM)
- Portable media players and handheld mobile devices

The figure above presents a streaming application scenario with the Montium core configured to perform DCT calculations. Utilizing parallelism and high-rate data transfers for both I/O and data processing guarantees minimal processing times in combination with very low power consumption.

Performance

Cycle count measures for a 2048-point IMDCT implemented on various platforms show that the Montium implementation outperforms conventional DSP architectures by a factor of ten. It also provides computation efficiency similar to dedicated ASIC and FPGA solutions.

Cycle counts for a 2048-point IMDCT

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