Fault-tolerant, adaptive Network-on-Chip IP

Product brief

Highlights

- Network-on-Chip interconnect technology
  - Scalable, deterministic, predictable, deadlock-free
  - Fault tolerant by design
  - AMBA 2 compatible

Target applications

- Heterogeneous multi-core architecture
  - Reliable data payload processing in space
  - Any application that requires highly reliable component interconnects

NoC IP – Network-on-Chip IP

The fault-tolerant Network-on-Chip IP is specifically designed to quickly and reliably route data from core to core in multi- and many-core System-on-Chips (SoCs) that are used in extreme conditions.

The NoC IP implements packet-switched NoC technology using dimensional XY-routing and wormhole switching in a two-dimensional mesh network.

The NoC IP implements fault-tolerance techniques and combines the determinism of XY-routing with explicitly programmable adaptiveness to provide a controlled manner for routing traffic around congested or faulty network elements, while preserving determinism and deadlock-freedom.

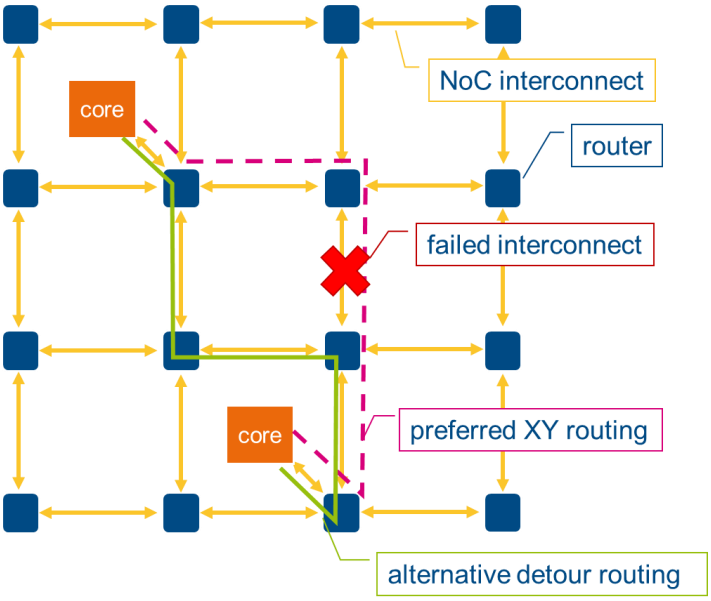
Key features

Network-on-Chip

- 32-bit packet-switched 2D-mesh network
- XY-routing, deadlock-free
- 5-port Routers featuring 4 prioritized services (using virtual channels)
- Quality of Service provided by prioritized services
- 32-bit data transfer per NoC link (per single direction)

Fault-resilient, reliable and adaptive

- Adaptive XY-routing provides data rerouting in the NoC in case of congestion or permanent connection errors.
- Flit-level flow control for more robust error signaling.
- Enable the insertion of EDAC for transient error protection on data links to increase robustness of data.



Fault-tolerant, adaptive NoC with data rerouting after a detected interconnect failure.

Network-on-Chip protocol packets

- Single read/write transactions
- Block read/write transactions
- Interrupt packet signaling
- Support for Indirect transactions (i.e. slave-to-slave operations using DMA controller)

Network-on-Chip Interfaces

- Network Interfaces connect IP components to the Local port of the NoC Router, such as
  - SpaceWire interfaces,
  - ADC & DAC converters,
  - Recore's Xentium DSP,
  - AMBA 2 compatible building blocks, e.g. GRLIB IP.

AMBA Network Interface – AMBA NI

- Transparent interfacing between NoC and AMBA domain
  - Access to memory-mapped I/O on NoC
  - 32-bit AHB-lite master/slave ports
- Interrupt signaling interface for NoC interrupt packets
- Interrupt signaling and forwarding of devices to NoC

Clock and Reset

- Single NoC clock domain
- Synchronous reset input

RECORE

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Easy to use NoC IP package

The NoC IP is technology agnostic, and can be synthesized for FPGA and ASIC.

The IP package comprises a complete IP package with VHDL sources, testbenches for the **NoC Router** and **AMBA Network Interface**, scripting, and documentation. It is further complemented by functional SystemC models, traffic monitoring configurations and scripting for throughput performance analysis.

A reference 3x3 NoC-mesh multi-core architecture is available for NoC IP validation on FPGA platforms.

The IP package contains:

- Configurable VHDL of **NoC Router**, including stand-alone testbench;
- Configurable VHDL of **AMBA NI**, including stand-alone testbench;
- SystemC model for early software development.

IP blocks

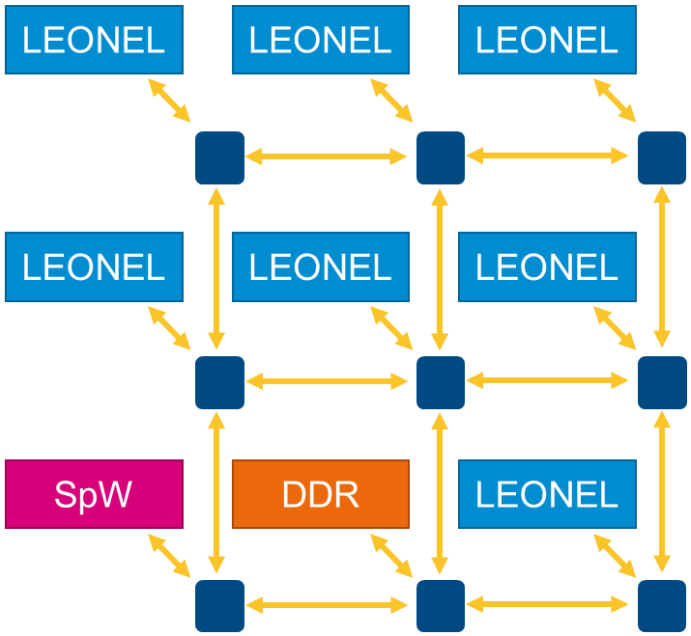
The main IP building blocks of a scalable Network-on-Chip are the **Router** IP and the **AMBA Network Interface** IP.

- **Router** IP: Using the North, East, South and West ports of the 5-port **Router** IP block it is straightforward to instantiate a 2D-mesh network.
- **AMBA NI** IP: The **AMBA Network Interface** provides AHB master and AHB slave interfacing for connecting IP components to the Local port of the 5-port **NoC Routers**.
  Using the **AMBA NI** one can easily connect AMBA AHB-based IP blocks in a memory-mapped NoC architecture.

Area/speed

The NoC IP runs at 180 MHz, 500 MHz and 1 GHz clock frequency in DARE180, C65SPACE and FDSOI28 ASIC technology, respectively.

The logic area of the **NoC Router** is estimated ~25 kGates (i.e. NoC Router with all ports connected).
The logic area of the complete **AMBA Network Interface** is estimated ~70 kGates (i.e. full version with both AHB master port and AHB slave port enabled).



3x3 NoC-mesh customer case with 7 LEON processing elements (LEONEL), SpaceWire interface and DDR memory controller integrated in the NoC.

For Xilinx Virtex-4 devices the following logic sizes are reported:

NoC Router: 2854 - 4637 Slices, 2316 - 3541 LUTs
AMBA NI: 4963 - 5996 Slices, 6910 - 7265 LUTs

Customer case

The NoC IP has been validated in a 3x3 NoC-mesh platform with multiple LEON3FT processing elements in FPGA. The 3x3 NoC-mesh multi-core platform runs at 40 MHz clock frequency in a Virtex-4 device. This FPGA-based platform has been validated while running parallelized JPEG compression software, spreading work over several processing elements.

The NoC IP building blocks allow for easily developing heterogeneous multi-core processor architectures.

For more details contact Gerard Rauwerda, CTO:
Gerard.Rauwerda@recoresystems.com

Recore Systems BV
PO Box 77
7500 AB Enschede
The Netherlands
☏ +31 53 4753 000
🖷 +31 53 4753 009
@ info@recoresystems.com