Multicore DSP unit prototype for sensor data processing in space

Product brief

Payload unit for data processing in space

Based on Recore Systems' multicore Digital Signal Processor (DSP) subsystem IP, the "Massively Parallel Processor Breadboarding (MPPB) Study" (ESA Contract No. 21986) developed a scalable heterogeneous multicore System-on-Chip (SoC) architecture and a payload unit prototype for future sensor data processing in space applications.

The payload unit prototype implements an instantiation of the SoC architecture on a Xilinx Virtex-5LX330T FPGA.
All functional interfaces are available on the front-panel of the MPPB unit, such as LCD, SpaceWire, ADC input interface, DAC output interface, debug and program interface, and general purpose IO.

The payload unit prototype features include:

Multicore SoC payload unit (2 units in picture)

Xentium DSP processors

- Two Xentium DSP tiles, with (per tile):
- Programmable high-performance fixed-point DSP core
- 200 16-bit MMACs/s; 100 32-bit MMACs/s (@50MHz)
- 100 16-bit complex MMACs/s (@50MHz)
- VLIW architecture with ten parallel execution units
- 32-bit and 40-bit scalar, and 16-bit vector operations
- 32 kByte data memory and 16 kByte instruction cache
- Two 64-bit local data memory buses and network IF bridge
- 32-bit instruction bus to network interface

LEON2 microprocessor

- 32-bit processor conforming to the IEEE® 1754 Sparc V8

Memories

- 256kB SRAM on the NoC
- 256MB DDR (@ 150MHz) on the NoC
- 256MB DDR (@ 150MHz) on the AHB
- 1GB Nand Flash on the AHB

Network-on-chip

- 32-bit packet-switched 2D Mesh network
- 5-port routers with 4 services
- 1.6 Gbps per link (@ 50 MHz) (per single direction)

ADC

- Analog Devices AD6644
- 14-bit resolution, 40 Msps

DAC

- Texas Instruments DAC5662
- 12-bit resolution, 40 Msps

SpaceWire interfaces

- Two 100Mbps Spacewire interfaces on NoC
- One 100 Mbps Spacewire interface with RMAP on AHB

Miscellaneous interfaces

- 16 GPIO, 2 UART, LCD with 2 lines of 16 characters
- Real Time Clock
- 2 24-bit timers and Watchdog

DMA

- DMA controller for 2D memory transfers with strides
- DMA in IO for SpaceWire and ADC/DAC interfaces

Multicore debugging

- LEON Debug Support Unit (DSU)
- Xentium Debug Unit; for each core
- Cross Trigger Unit for programmable stop and resume triggering of multiple cores
- Xentium-gdb and GRMON support via DCOM UART link

Xentium performance counters

- One 48-bit clock cycle counter (per core)
- 4 32-bit general configurable event counters (per core)

Clock and Reset Manager (CRM)

- PLL 50MHz to 75MHz, 100MHz, 150MHz and 200MHz
- Internal power-up reset generation
- JTAG reset, Watchdog
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required power supplies: 12V external DC input power

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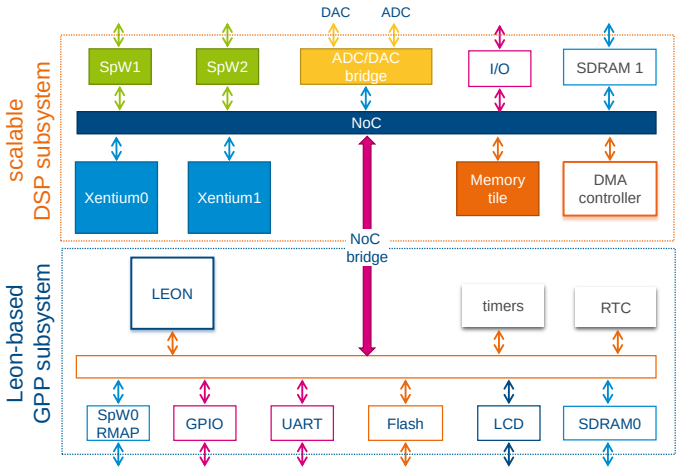
Heterogeneous, scalable multicore DSP

The developed multicore DSP SoC architecture combines the benefits of heterogeneity and integration in a scalable and energy-efficient architecture.

The architecture includes Recore's scalable DSP subsystem and a General-Purpose Processor (GPP) system. The DSP subsystem is a customization of Recore's multicore DSP subsystem IP based on Xentium® DSP processors in a Network-on-Chip (NoC). The GPP subsystem is based on Cobham Gaisler's LEON2 microprocessor with a conventional bus subsystem.



Architecture

The architecture comprises a System-on-Chip integrating on one chip multiple processing cores with SpaceWire (including RMAP protocol support), CCSDS timers, ADC/DAC interfaces, and on-chip as well as off-chip memories. In general, data interfaces are connected directly to the NoC of the DSP subsystem and control interfaces and peripherals are placed on the bus of the GPP subsystem.

Firmware upgrade for evaluation of new DSP IP features

A firmware upgrade of the MPPB unit is available for evaluation of new candidate IP features for the Scalable Sensor Data Processor (SSDP) IC under development. The new firmware can be used with the existing HW configuration. The upgrade improves programmability with amongst others Xentium multicore debugging, Xentium performance counters, and additional DMA features.

Commercial availability

Both Xentium IP and NoC IP are available from Recore Systems. For more details see www.recoresystems.com.
To test your target applications on the functional prototype ESA offers evaluation opportunities. To develop applications, you need a license for the accompanying Software Development Environment (SDE) from Recore Systems.

For more details contact Gerard Rauwerda, CTO,
Gerard.Rauwerda@recoresystems.com

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Recore Systems BV
PO Box 77
7500 AB Enschede
The Netherlands
☎ +31 53 4753 000
🖷 +31 53 4753 009
@ info@recoresystems.com