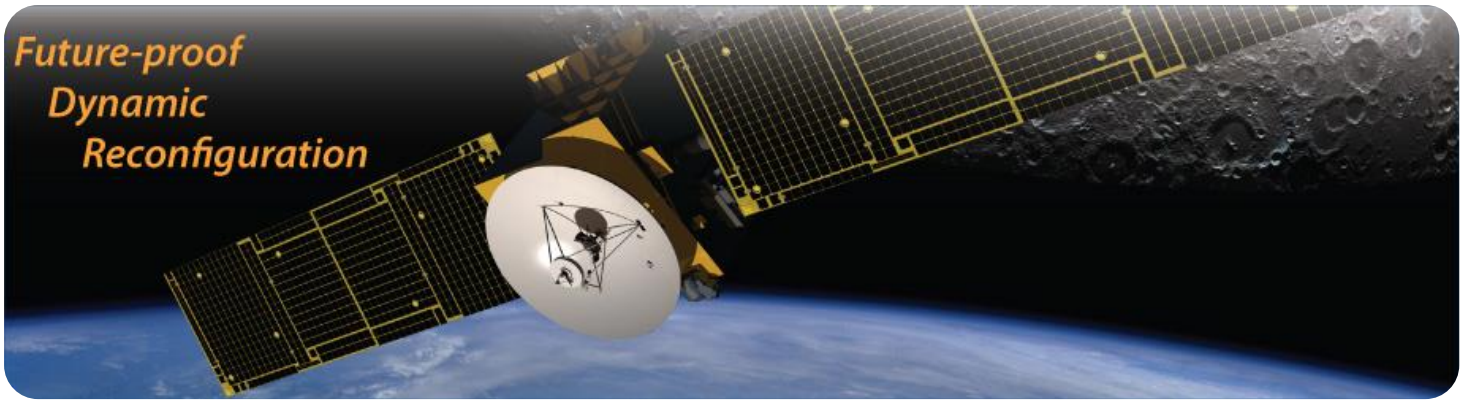
RECORE

Reliable data processing for space applications



A reliable data processor for space

In close cooperation with and in assignment of the European Space Agency ESA, we have been developing reliable, fault-tolerant, radiation-resistant data processor IP for on-board sensor data processing with state-of-the-art processing power. We used a stepwise approach and developed various prototypes with our IP inside:

1. A functional prototype combining new fault-tolerance techniques with proven space components
2. Rad.-hard silicon prototype with crucial IP
3. Multi-core Scalable Sensor Data Processor for space.

To boldly go… and send reliable data to earth

Everyone in the space industry is very much aware of the data-corrupting consequences of radiation in deep space, and will only use radiation-hard components for space missions.

On scientific missions to deep space a wealth of data is gathered, analyzed and compressed on-board before being relayed back to earth. The data cannot be sent to earth in its entirety since modern instruments gather much more data than can be communicated back to earth. For a correct interpretation of what is going on in space, and valid answers to exciting questions it is key that the compressed and processed data is correct.

Unfortunately, reliably processing and compressing of data might be easier said than done, as the only existing European digital signal processor (DSP) for space is obsolete: it provides less than 6% of the 1000 MFLOPS performance expected today. European space missions currently rely on a combination of FPGAs and commercial off-the-shelf (COTS) components, with the drawbacks of limited reliability and significant extra mass, complexity, and power consumption.

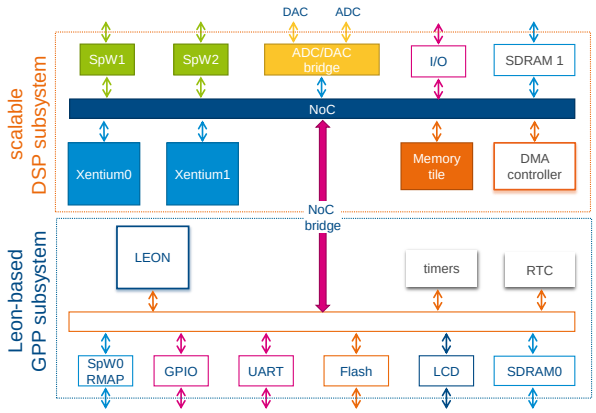
With the planning for the Cosmic Vision programme in mind, ESA plans to have a standard ASIC with a space qualified rad-hard Digital Signal Processor and a performance of at least 1000 MFLOPS in its portfolio.

Step 1: Functional prototype

As a first step, we developed a functional prototype of a reliable data processor for space missions based on our Xentium DSP IP and Network-on-Chip IP.

The prototype can withstand radiation-induced data errors both on the software and hardware level. It combines ideas for self-repairing chips with existing space-proven components such as SpaceWire.

Crucial architectural details:



- 2 Xentium DSPs (fixed point)
- 1 LEON processor
- 256 kB on-chip memory tile and off-chip memory
- SpaceWire interfaces
- ADC/DAC interfaces
- Network on Chip (NoC)
- Memory mapped communication protocol

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Step 2: Rad-hard silicon prototype

As a second step on the road to a reliable data processor, key parts of the functional prototype design were hardened in 180nm CMOS technology, using the IMEC DARE libraries.

Hardened IP components in prototype ASIC

- Xentium DSP IP core @ 100MHz
- Network-on-Chip IP
- SpaceWire (SpW-RMAP) and ADC/DAC interfaces
- Small on-chip memory tile
- Watchdog timer

Radiation Hardening

- DARE 180nm CMOS technology
- EDAC protected SRAMs

Irradiation Testing

The ASIC prototype has undergone functional testing under full radiation.

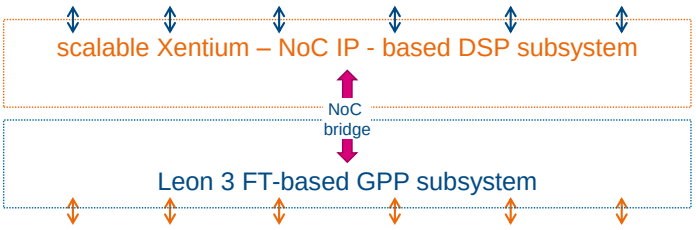
- SEL: > 70 MeV/cm^2/mg
- SEE – SEU: > 50 MeV/cm^2/mg

Step 3: Scalable Sensor Data Processor (SSDP)

Currently, a consortium of renowned partners in the space industry brings together the functional and rad-hard silicon prototypes in a high performance, scalable, rad-hard (~1 Mrad TID), highly integrated mixed-signal Data Processor for Sensors, Instruments, and Processing Units with excellent re-use potential for future Science & Exploration missions.

Architectural details:

The SSDP data processor combines a fault-tolerant LEON3FT-based General Purpose Processor subsystem



with a Xentium-NoC-based DSP subsystem. The architecture is similar to that of the functional prototype in step 1.

Commercial availability

Both Xentium and NoC IP are available via Recore Systems. For more details see www.recoresystems.com.
To test your target applications on the functional prototype ESA offers evaluation opportunities. To develop applications, you need a license for the accompanying Software Development Environment (SDE) via Recore Systems.
Packaged and functionally tested prototype SSDP ASICs, suitable for prototype / EM systems, instruments, and data processing units, are expected to be available in 2017.

For more details contact Gerard Rauwerda, CTO,
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What's up next?

The journey of integrating more Xentium DSP cores in the DSP subsystem will continue to further increase the performance of the data processor and floating-point functionality will be added. The next expected step is a many-core floating-point DSP subsystem. This will increase both performance and reliability of the data processor. So we can boldly go and send reliable data to earth!

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